Isolated Sigma-Delta Modulator

Preliminary Technical Data

AD7400/AD7401

FEATURES

- Up to 20 MHz Data Rate (AD7401)
- 10 MHz Data Rate (AD7400)
- 2nd Order Modulator
- ±4 LSB INL @16 Bits
- Onboard Digital Isolator
- Onboard Reference
- Low Power Operation:
  - 15 mA @ 5 V
- -40°C to +105°C Operating Range
- 16-ld SOIC Package
- Safety and Regulatory Approvals
  - UL Recognition
    - 3750 V_{RMS} for 1 minute per UL 1577
  - CSA Component Acceptance Notice ~5A
  - VDE Certificate of Conformity
    - DIN EN 60747-5-2 (VDE 0884 Part 2):2003-01
    - DIN EN 60950 (VDE 0805): 2001-12; EN 60950:2000
    - V_{IORM} = 840V_{PEAK}

APPLICATIONS

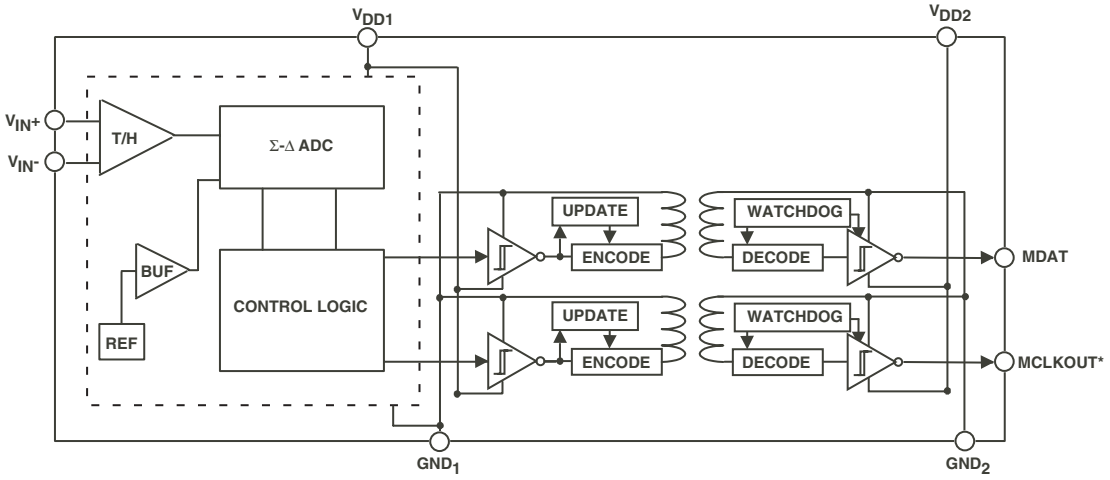
- AC Motor Control
- Data Acquisition Systems
- A/D + Opto-Isolator Replacement

GENERAL DESCRIPTION

The AD7400/AD7401 are 2nd order sigma-delta modulators that convert an analog input signal into a high speed 1-bit data stream with onboard digital isolation based on Analog Devices' *i*Coupler® technology. The AD7400/AD7401 operate from a 5 V power supply and accept a differential input signal of ±200 mV. The analog input is continuously sampled by the analog modulator, eliminating the need for external sample and hold circuitry. The input information is contained in the output stream as a density of ones with data rates up to 20MHz. The original information can be reconstructed with an appropriate digital filter. The serial I/O may use a 5V or 3V supply (V_{DD2}).

The serial interface is digitally isolated. High-speed CMOS,

FUNCTIONAL BLOCK DIAGRAM



*MCLKIN pin on AD7401

Rev. PrJ

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combined with monolithic air core transformer technology, means the onboard isolation provides outstanding performance characteristics superior to alternatives such as optocoupler devices. The parts provide an on-chip 2.5V reference. The AD7400/AD7401 are offered in a 16-lead SOIC package and have an operating temperature range of -40°C to +105°C.

TABLE OF CONTENTS

REVISION HISTORY

Revision PrJ: Preliminary Version

AD7400—SPECIFICATIONS[1]

Table 1. (V_{DD1} = V_{DD2} = 4.5V to 5.5V, , V_{IN}+ = -200mV to +200mV and V_{IN}- = 0V; T_A = T_{MIN} to T_{MAX}, f_{MCLK} = 10MHz unless otherwise noted.)

Parameter	B Version[1,5]	Units	Test Conditions/Comments
STATIC PERFORMANCE			When Tested with Sinc[3] Filter[4]
Resolution	16	Bits min	Filter output truncated to 16 Bits
Integral Nonlinearity[2]	±4	LSB max	
Differential Nonlinearity[2]	±0.9	LSB max	Guaranteed No Missed Codes to 15 bits
Offset Error[2]	±0.5	mV max	Bipolar Input Range
Offset Drift vs. Temperature[2]	5	µV/°C max	
	2	µV/°C typ	
Offset Drift vs. V_{DD1}[2]	0.05	mV/V typ	
Absolute Reference Voltage Tolerance	±1	%min/max	
V_{REF} Drift vs. Temperature[2]	60	ppm/°C typ	
V_{REF} Drift vs. V_{DD1}[2]	0.2	% typ	
ANALOG INPUT			
Input Voltage Range	±200	mV min/max	For specified performance. Full range ±320mV.
DC Leakage Current	±1	µA max	
DYNAMIC SPECIFICATIONS			When Tested with Sinc[3] Filter[4]
Signal to Noise + Distortion Ratio (SINAD)[2]	70	dBmin	V_{IN}+ = 21Hz, 400mV_{pk-pk} sine wave
	76	dB typ	
Total Harmonic Distortion (THD)[2]	-80	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	-80	dB typ	
Effective number of bits	12	Bits	
Isolation Transient Immunity	15	kV/µs min	
	20	kV/µs typ	
Signal Delay	20	µs typ	Delay through filter varies with actual value of on-board clock. Decimation by 256.
	24	µs max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD2} – 0.1	V min	I_O = -20 µA
Output Low Voltage, V_{OL}	0.4	V max	I_O = 20 µA
POWER REQUIREMENTS			
V_{DD1}	+4.5/+5.5	Vmin/Vmax	
V_{DD2}	+4.5/+5.5	Vmin/Vmax	
	+2.7/+3.3	Vmin/Vmax	
I_{DD1}[7]	18	mA max	V_{DD1} = 5.5V
I_{DD2}[7]	5	mA max	V_{DD2} = 5.5V

NOTES
[1] Temperature ranges as follows: -40°C to +105°C
[2] See Terminology section.
[3] Sample tested @ 25°C to ensure compliance.
[4] Filter as defined by Verilog Code.
[5] All voltages are relative to their respective ground.
Specifications subject to change without notice.

AD7401—SPECIFICATIONS[3]

Table 2. (V_{DD1} = V_{DD2} = 4.5V to 5.5V, , V_{IN}+ = -200mV to +200mV and V_{IN}- = 0V; T_A = T_{MIN} to T_{MAX}, f_{MCLK} = 20MHz unless otherwise noted.)

Parameter	B Version[1,5]	Units	Test Conditions/Comments
STATIC PERFORMANCE			When Tested with Sinc[3] Filter[4]
Resolution	16	Bits min	Filter output truncated to 16 Bits
Integral Nonlinearity[2]	±4	LSB max	
Differential Nonlinearity[2]	±0.9	LSB max	Guaranteed No Missed Codes to 15 bits
Offset Error[2]	±0.5	mV max	Bipolar Input Range
Offset Drift vs. Temperature[2]	5	µV/°C max	
	2	µV/°C typ	
Offset Drift vs. V_{DD1}[2]	0.05	mV/V typ	
Absolute Reference Voltage Tolerance	±1	%min/max	
V_{REF} Drift vs. Temperature[2]	60	ppm/°C typ	
V_{REF} Drift vs. V_{DD1}[2]	0.2	% typ	
ANALOG INPUT			
Input Voltage Range	±200	mV min/max	For specified performance. Full range ±320mV.
DC Leakage Current	±1	µA max	
DYNAMIC SPECIFICATIONS			When Tested with Sinc[3] Filter[4]
Signal to Noise + Distortion Ratio (SINAD)[4]	70	dBmin	V_{IN}+ = 21Hz, 400mV_{pk-pk} sine wave
	76	dB typ	
Total Harmonic Distortion (THD)[2]	-80	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	-80	dB typ	
Effective number of bits	12	Bits	
Isolation Transient Immunity	15	kV/µs min	
	20	kV/µs typ	
Signal Delay	10	µs typ	Delay through filter varies with actual value of external clock. Decimation by 256.
	12	µs max	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	µA max	
Input Capacitance, C_{IN}[3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD2} – 0.1	V min	I_O = -20 µA
Output Low Voltage, V_{OL}	0.4	V max	I_O = 20 µA
POWER REQUIREMENTS			
V_{DD1}	+4.5/+5.5	Vmin/Vmax	
V_{DD2}	+4.5/+5.5	Vmin/Vmax	
	+2.7/+3.3	Vmin/Vmax	
I_{DD1}[7]	21.2	mA max	V_{DD1} = 5.5V
I_{DD2}[7]	3.92	mA max	V_{DD1} = 5.5V, Digital I/Ps = 0 V or V_{DD1}

NOTES
[3] Temperature ranges as follows: -40°C to +105°C
[4] See Terminology section.
[3] Sample tested @ 25°C to ensure compliance.
[4] Filter as defined by Verilog Code.
[5] All voltages are relative to their respective ground.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1]

Table 3. AD7400/AD7401 Timing Specifications (V_{DD1} = V_{DD2} = 4.5V to 5.5V, T_A = T_{MAX} to T_{MIN} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
$F_{MCLKOUT}$	10	MHz typ	AD7400
	8.2/13.2	MHz min/max	
T_{MCLKIN}[2]	1	MHz min	AD7401
	20	MHz max	
t_1[3]	30	ns max	Data Access Time after MCLK Rising Edge
t_2[3]	15	ns min	Data Hold Time after MCLK Rising Edge
t_3	0.4 x t_{MCLKIN}	ns max	Master Clock Low Time
t_4	0.4 x t_{MCLKIN}	ns max	Master Clock High Time

NOTES

[1] Sample tested @ 25°C to ensure compliance. All input signals are specified with tr = tf = 5ns (10% to 90% of V_{DD1}) and timed form a voltage level of 1.6 Volts. See Figure 1.

[2] Mark Space ratio for the MCLKIN input is 40/60 to 60/40.

[3] Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8V or 2.0V.

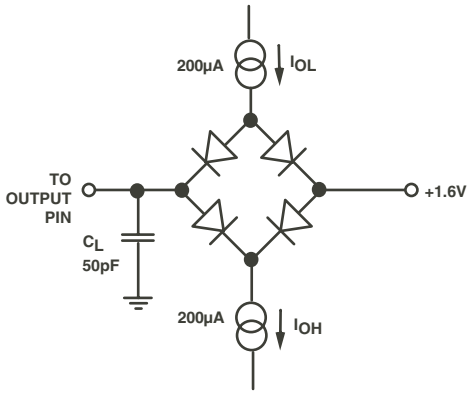


Figure 1. Load Circuit for Digital Output Timing Specifications

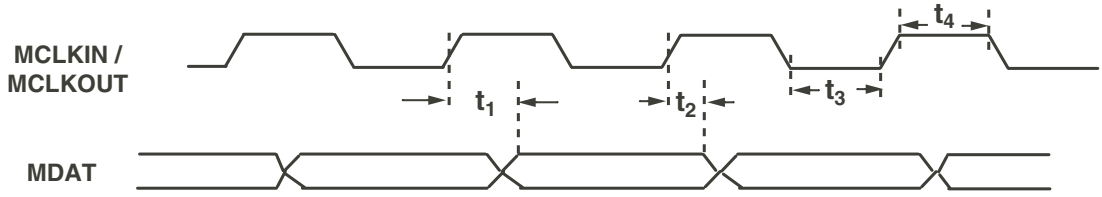


Figure 2. Data Timing

ABSOLUTE MAXIMUM RATINGS[1,3]

Table 4. AD7400/AD7401 Absolute Maximum Ratings (T_A = +25°C unless otherwise noted)

V_{DD1} to GND_1	-0.3 V to +6.5V
V_{DD2} to GND_2	-0.3 V to +6.5 V
Analog Input Voltage to GND_1	-0.3 V to V_{DD1} +0.3V
Digital Input Voltage to GND_2	-0.3 V to V_{DD2} +0.5 V
Output Voltage to GND_2	-0.3 V to V_{DD2} +0.3V
Input Current to Any Pin Except Supplies[2]	±10mA
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
SOIC Package	
θ_{JA} Thermal Impedance	89.2 °C/W
θ_{JC} Thermal Impedance	55.6 °C/W
Resistance (Input-Output), R_{I-O}	$10^{12}\Omega$
Capacitance (Input-Output), C_{I-O}	1pF
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infared (15 sec)	+220°C
ESD	TBD

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100mA will not cause SCR latch up.

[3] All voltages are relative to their respective ground.

REGULATORY INFORMATION (PENDING)

Table 5. Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Input-Output Withstand Momentary Withstand Voltage[1]	V_{ISO}	3750 min.	V	Note 1
Minimum External Air Gap (Clearance)	L(I01)	8.4 min	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Gap (Internal Clearance)		0.025 min	mm	Insulation distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110,1/89,Table 1)

UL[1]	CSA	VDE[2]
Recognized under 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2):2003-01[2]
Double insulation, 3750 V rms isolation voltage	Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 630 V rms maximum working voltage	Basic insulation, 891 V peak Complies with DIN EN 60747-5-2 (VDE 0884 Part 2):2003-01, DIN EN 60950 (VDE 0805):2001-12; EN 60950:2000 Reinforced insulation, 891 V peak

NOTES

[1] In accordance with UL1577, each AD7400/AD7401 is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (current leakage detection limit = 10 µA).

[2] In accordance with DIN EN 60747-5-2, each AD7400/AD7401 is proof tested by applying an insulation test voltage ≥ 1670 V peak for 1 second (partial discharge detection limit = 5 pC).

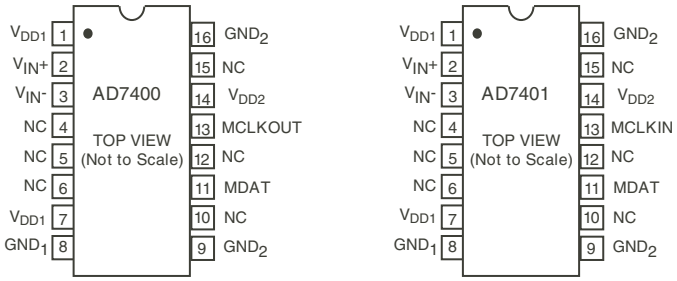
DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS (PENDING)

Table 6.

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110			
For Rated Mains Voltage ≤ 300 V rms		I–IV	
For Rated Mains Voltage ≤ 600 V rms		I–III	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	V_{IORM}	891	Vpeak
Input to Output Test Voltage, Method b1	V_{PR}	1670	V peak
$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC			
Input to Output Test Voltage, Method a	V_{PR}		
After Environmental Tests Subgroup 1)		1426	Vpeak
$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5p C			
After Input and/or Safety Test Subgroup 2/3)		1069	Vpeak
$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5p C			
Highest Allowable Overvoltage	V_{TR}	6000	V peak
(Transient Overvoltage, t_{TR} = 10 sec)			
Safety-Limiting Values (Maximum value allowed in the event of a failure, also see Thermal Derating Curve)			
Case Temperature	T_S	150	°C
Side 1 Current	I_{S1}	TBD	mA
Side 2 Current	I_{S2}	TBD	mA
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

This isolator is suitable for "basic electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

"*" marking on packages denotes DIN EN 60747-5-2 approval for 891 V peak working voltage.



Pin Functional Descriptions

Table 7. AD7400/AD7401 Pin Function Descriptions

Pin Number	AD7400 Pin Mnemonic	AD7401 Pin Mnemonic	Description
1,7	V_{DD1}	V_{DD1}	Supply Voltage, 5 V ±10%. This is the supply voltage for the isolated side of the AD7400/AD7401 and is relative to GND_1.
2	$V_{IN}+$	$V_{IN}+$	Positive analog Input, range of ±200 mV .
3	$V_{IN}-$	$V_{IN}-$	Negative analog input (normally connected to GND_1).
11	MDAT	MDAT	Serial Data Output. The single bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKIN/MCLKOUT input.
13		MCLKIN	Master Clock. Logic Input. An external clock is applied at this pin. A serial clock input from 1MHz to 20MHz may be applied to this pin on the AD7401. The bit stream form the modultaor is valid on the rising edge of MCLKIN.
13	MCLKOUT		Master Clock. Logic Output, 10MHz typical. The bit stream form the modultaor is valid on the rising edge of MCLKOUT on the AD7400.
14	V_{DD2}	V_{DD2}	Supply Voltage, 5 V ±10% or 3V ±10%. This is the supply voltage for the non-isolated side of the AD7400/AD7401 and is relative to GND_2.
8	GND_1	GND_1	Ground. This is the ground reference point for all circuitry on the isolated side of the AD7400/AD7401.
9,16	GND_2	GND_2	Ground. This is the ground reference point for all circuitry on the non-isolated side of the AD7400/AD7401.
4-6,10,12,15	NC	NC	No Connect

Theory of Operation

CIRCUIT INFORMATION

The AD7400/AD7401 Isolated Sigma-Delta Modulator converts an analog input signal into a high-speed, (10MHz using on-board MCLK on AD7400, or up to 20MHz using external MCLK on AD7401), single-bit data stream; the time average of the modulator's single-bit data is directly proportional to the input signal. Figure 4 shows a typical application circuit where the AD7400/AD7401 is used to provide isolation between the analog input, a current sensing resistor, and the digital output which is then processed by a digital filter to provide an N-bit word.

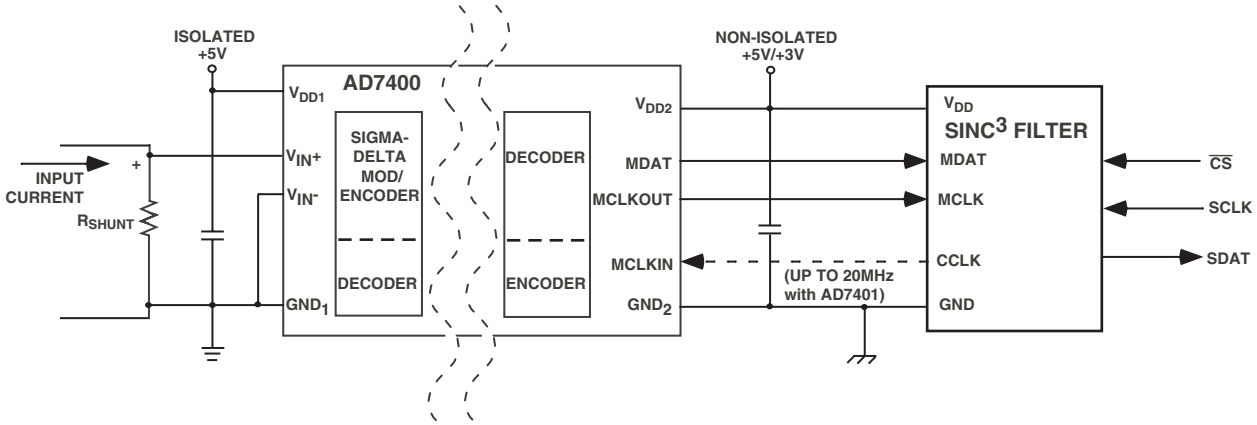


Figure 4. Typical Application Circuit

ANALOG INPUT

The differential analog input of the AD7400/AD7401 is implemented with a switched capacitor circuit. This circuit implements a 2nd-order modulator stage which digitizes the input signal into a 1-bit output stream. The sample clock (MCLK) provides the clock signal for the conversion process as well as the output data-framing clock. This clock source is internal on the AD7400 and external on the AD7401. In the case of the AD7401 different clock frequencies allow for a variety of solutions and signal bandwidths or for accurate synchronization of several AD7401 devices used in the same system.

The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream which accurately represents the analog input over time appears at the output of the converter. See figure x.

Table 8. Analog Input Range

Analog Input	Voltage Input
Full Scale Range	640 mV
+Full Scale	+320 mV
+ Specified Input range	+200 mV
Zero	0 mV
-Specified Input range	-200 mV
-Full Scale	-320mV

OUTLINE DIMENSIONS

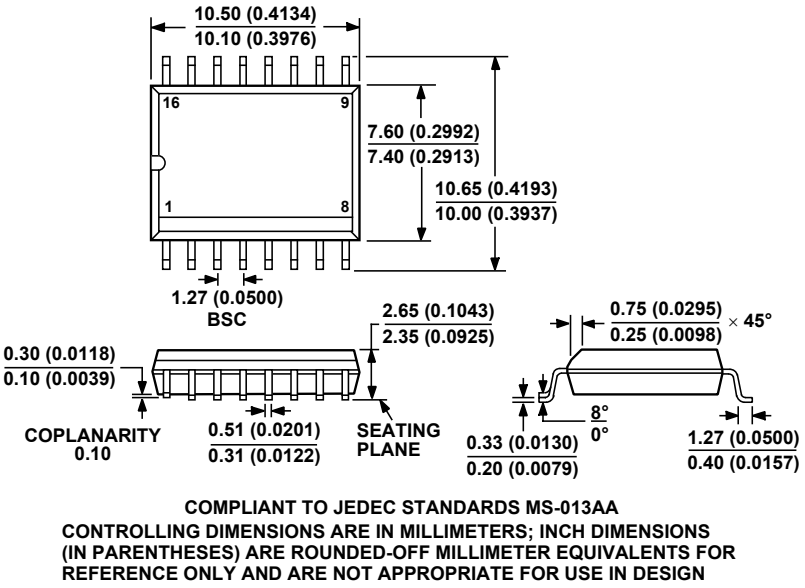


Figure 2. 16-Lead Short Outline Package [SOIC] Wide Body (RW-16)—Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Ordering Guide

AD7266 Products	Temperature Package	Package Description	Package Outline
AD7400YRWZ	–40°C to +105°C	Short Outline I.C. Package	RW-16
AD7400YRWZ-REEL	–40°C to +105°C	Short Outline I.C. Package	RW-16
AD7400YRWZ-REEL7	–40°C to +105°C	Short Outline I.C. Package	RW-16
AD7401YRWZ	–40°C to +105°C	Short Outline I.C. Package	RW-16
AD7401YRWZ-REEL	–40°C to +105°C	Short Outline I.C. Package	RW-16
AD7401YRWZ-REEL7	–40°C to +105°C	Short Outline I.C. Package	RW-16

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